Exhibit 58

No. 21-1772

United States Court of Appeals for the Federal Circuit

ACQIS, LLC,

Plaintiff-Appellant,

– v. –

EMC CORPORATION,

Defendant-Appellee.

Appeal from the United States District Court
for the District of Massachusetts, No. 1:14-cv-13560-ADB,
Hon. Allison Dale Burroughs

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INTRODUCTION

The primary dispute is whether a "transaction in accordance with the … PCI Local Bus Specification" refers to the *instructions* that tell a PCI component what to do (ACQIS's position) or instead, those instructions *plus* the signals for *transporting* those instructions to the PCI component over a parallel PCI bus (EMC's position).

Resolving the dispute requires analyzing the PCI Specification and competing expert reports to determine how a skilled artisan would have understood the Specification's description of a "transaction." The district court refused to perform that analysis at summary judgment because it believed that ACQIS had waived the issue by failing to raise it earlier. That was error.

EMC does not defend that error. Instead, it argues that the district court actually refused to hear ACQIS's claim construction argument for a *different* reason: because the district court had already heard and rejected ACQIS's argument at claim construction. But that is neither what the order holds nor what actually happened.

Because it is undisputed that the district court was wrong about waiver, this Court should (at least) vacate summary judgment and remand the claim construction dispute for resolution by the district court in the first instance. Alternatively, the Court can analyze the PCI Specification and expert reports to resolve the dispute on appeal.

Either way, the Court should at least reverse summary judgment against the Address and Data Claims. EMC argues that ACQIS never sought different treatment for those claims, but the record (including EMC's own briefing) shows otherwise. On the merits, EMC argues that the Address and Data Claims still require a *full* PCI bus transaction, despite reciting only the "address and data bits," but that argument contradicts the claim language.

Finally, the Court should side with ACQIS on the non-dispositive claim construction issues—*i.e.*, "communicating" and "encod[ing]" a transaction. EMC does not disagree that "communicating" a transaction requires communicating only the information that comprises the "transaction," as ACQIS argued, and that is sufficient reason to adopt ACQIS's position. On "encoded," EMC argues that (1) the construction *is* dispositive and (2) the district court was correct to require that "transactions" always be "encoded" *from parallel signals* (rather than from memory). Both propositions are wrong: (1) the district court's construction of "encoded" is non-dispositive because summary judgment rested solely on the construction of "PCI bus transaction," and (2) that construction is based on a purported disclaimer that ACQIS never made.

ARGUMENT

I. The district court erred by granting summary judgment based on an incorrect construction of "PCI bus transaction."

EMC's failure to defend the district court's holding of waiver is itself compelling reason to vacate and remand. But if the Court does decide to reach the merits, it should hold that a "transaction in accordance with the … PCI Local Bus Specification" requires only the instructions that tell the PCI component what to do (*i.e.*, the operation to perform), not the physical layer signals used to transport that transaction (such as control signals and parity bits). Finally, even if a "transaction" were to include that extra information, the "address and data bits" of the transaction do not.

A. EMC does not defend the district court's finding of waiver.

EMC does not dispute ACQIS's lead argument: that "[t]he district court erred *procedurally* by refusing to consider ACQIS's claim interpretation arguments as purportedly untimely and therefore waived." ACQIS Br. 33. That alone is sufficient to vacate and remand.

Rather than defend the actual order on appeal, EMC posits a hypothetical order in which the district court did not find *waiver*, but instead refused to "rehear the same arguments that it already rejected" at claim construction. EMC Br. 41-44. That argument has two serious problems.

First, the summary judgment order is based on *waiver*, not refusal to "re-hear" previously rejected arguments. EMC Br. 44. *Second*, the district court did *not* reject ACQIS's summary judgment arguments at claim construction.

1. EMC defends reasoning not in the order.

As ACQIS explained (ACQIS Br. 33-44), the district court refused to consider ACQIS's summary judgment arguments because it held (incorrectly) that those arguments were "*untimely*." Appx9-10. That much is plain from the language of the order:

- "ACQIS had ample opportunity to argue for a modified definition of the Specification during either court's claim construction proceedings, but chose not to do so." Appx10.
- "ACQIS never sought to disavow the elements of the Specification pertaining to a physical bus." Appx9.
- "ACQIS never attempted to parse the Specification in order to differentiate the elements that describe the methodology of the PCI bus transaction from those that describe the substance of the transaction." *Id.*
- "[ACQIS] could (and should) have sought a construction to that effect." Appx10 (quoting *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 520 (Fed. Cir. 2012)).

- "Only now, at summary judgment, does ACQIS seek to disavow the parts of the Specification unfavorable to its infringement claims." Appx9.
- "ACQIS's attempt to reduce the import of the Specification is [therefore] untimely." Appx9.

Nowhere does the order reason that the district court had already heard and rejected ACQIS's arguments at claim construction.

On appeal, EMC does not dispute that ACQIS's summary judgment arguments were timely. To the contrary, EMC agrees that ACQIS had *always* argued that a "transaction" is limited to transaction-layer information. EMC Br. 43. It is therefore undisputed that ACQIS did not *waive* the claim interpretation arguments it presented at summary judgment, and the district court's finding of waiver was therefore an abuse of discretion. *AdjustaCam, LLC v. Newegg, Inc.*, 861 F.3d 1353, 1358 (Fed. Cir. 2017) ("A district court abuses its discretion when its ruling rests on an erroneous legal conclusion or on a clearly erroneous assessment of the evidence."). At a minimum, the Court should vacate and remand for the district court to consider ACQIS's claim interpretation arguments in the first instance.

2. The district court did not reject ACQIS's summary judgment arguments at claim construction.

Rather than defend the actual order on appeal, EMC posits that the order was not based on waiver, but on the district court's refusal to "rehear

the same arguments that it already rejected" at claim construction. EMC Br. 44. According to EMC, "[t]here was no 'new' claim construction dispute" at summary judgment. *Id.* at 43. Rather, the district court merely refused to "decide a dispute already resolved." *Id.* at 44.

EMC misreads both the order and the record. As shown above, the summary judgment order rejects ACQIS's arguments as *waived*, not as *old*. Moreover, in fact the district court did *not* hear and resolve those same arguments at claim construction. If it had, this Court would have a record of that decision to review. It would have fact findings about how a skilled artisan would have understood the term "transaction" in the context of the PCI Specification. It would also have the benefit of a trial court's legal interpretation of that Specification, its identification of the relevant portions, and its analysis of whether those portions demonstrate that a "transaction in accordance with" the PCI Specification must include "control signals" and "parity bits." That the record contains none of these things confirms that, contrary to EMC's argument, the district court did *not* previously analyze and reject ACQIS's claim interpretation arguments.

The primary dispute at claim construction was not what information a "transaction" contains, but whether a transaction must be communicated over a PCI Local Bus (as EMC argued). Appx1700-1704. EMC lost that

argument. *Id.* On what information constitutes the "transaction," the parties simply agreed that the transaction must be "in accordance with the PCI Standard." The parties did not ask the court to define what information this requires because the issue was not disputed. Appx1700. Consequently, the district court's *Markman* order does not address whether a "transaction" includes physical layer information. Appx1700-1704.

Judge Davis also did not resolve that issue. As in Massachusetts, the primary dispute before Judge Davis was whether the claims require a physical bus—not what information constitutes a transaction. Appx505-507. He too resolved that dispute for ACQIS. Appx505-507. On what information constitutes a "transaction," Judge Davis's *Markman* order did (in a single sentence) decline to "define a 'transaction' as digital command, address, and data information." Appx507. But the order does not explain what more or less a "transaction" must include or why. It merely holds that each type of transaction must be "in accordance with" whatever information the PCI Specification requires. *Id.* The order is silent on what information that is.

Thus, at *Markman*, Judge Davis declined to resolve (*as a matter of law*) what information the PCI Bus Specification requires for each type of transaction. Instead, he found it sufficient (at that stage) to assume that a jury could determine whether any transaction ultimately identified in the

accused product is "in accordance with the PCI standard." *Id.* If a legal dispute were to ripen about what information is required (as happened at summary judgment), the court could sharpen the construction then.

Thus, neither district court decided at claim construction that "accordance with the … PCI Local Bus Specification" requires physical layer "control signals" or "parity bits." That dispute surfaced for the first time at summary judgment. Appx3333-3334. ACQIS then asked the district court to resolve the dispute then (Appx3347-3359), but the court refused to hear ACQIS's side because it thought (incorrectly) that "district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs." Appx10. They are, and the district court's refusal was therefore an error of law. ACQIS Br. 39-44; *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it").

B. A "transaction in accordance with the … PCI Local Bus Specification" does not require physical layer signals.

If the Court reaches the merits of the claim construction dispute, it should hold that a "transaction in accordance with the … PCI Local Bus Specification" does *not* include the physical layer signals identified by EMC. ACQIS Br. 44-53. As ACQIS has shown, both the intrinsic and extrinsic

evidence support that conclusion. Rather than rebut that evidence, EMC reframes the dispute incorrectly and miscasts it as three separate issues.

1. EMC frames the dispute incorrectly.

EMC mistakenly describes ACQIS's argument as being that a "PCI bus transaction" must "compl[y] with *only a portion of* the PCI standard" (EMC Br. 41) (emphasis added), rather than with the standard "in its entirety" (*id.* at 28). Presumably, EMC does this to juxtapose that position with Judge Davis's comment that a transaction must "include *all information required by the PCI standard*" or with expert testimony that a PCI transaction must include "no less" than that information. EMC Br. 28 (emphasis EMC's) (quoting Appx507 and Appx924).

EMC's framing is misleading. The issue is not whether a transaction must comply with *all* of the PCI Specification's definition of a transaction, or only *some* of that definition. The issue is how the PCI Specification defines a *"transaction."* As ACQIS has shown, the Specification defines a "transaction" as the information that one PCI component actually passes to another to tell that other component what to do—not the signals used to shuttle that information over the parallel bus. ACQIS Br. 44-53.

2. The PCI Specification does not define a "transaction" to include physical layer signals.

On appeal, EMC makes what looks like three independent arguments: that a "transaction" must include (1) "control signals" (EMC Br. 30-38), (2) "parity signals" (*id.* at 38-40), and (3) "phases" (*id.* at 40-41). These are not independent arguments because each reduces to the same issue: whether a "transaction" must include the physical layer signals used to transport the transaction between devices. A "transaction" either includes all of those signals or none. The intrinsic and extrinsic records show that it includes none.

Ultimately, EMC simply rejects ACQIS's contention that the PCI Specification defines both a transaction layer and a physical layer. EMC Br. 29 ("the PCI Local Bus Specification does not divide the PCI standard into layers."). But this view contradicts expert testimony establishing that, while the PCI Specification does not use the term "layers," a skilled artisan would have nonetheless understood the PCI Specification to define a "transaction layer" *and* a "physical layer." Appx2469 (¶ 48); Appx2505; *see also* Appx3396-3406; Appx2602 (¶ 245). The district court articulated no findings of fact regarding that testimony or any legal analysis of the PCI Specification contradicting it. Given the procedural posture, the Court should accept that a skilled artisan would have understood the PCI Specification to

define transaction and physical layers. *See Sheinkopf v. Stone*, 927 F.2d 1259, 1262 (1st Cir. 1991) (the Court "must view the evidentiary record in the light most hospitable to the nonmovant and must indulge all reasonable inferences in his favor").

In light of this understanding, a "transaction" does not include any physical layer signals, including "control signals" (EMC Br. 30-38), "parity signals" (*id.* at 38-40), or "phases" (*id.* at 40-41).

a) Control signals

EMC dedicates most of its pages to arguing that a "transaction in accordance with the … PCI Local Bus specification" must include physical layer "control signals" (*i.e.*, the signals used to control a PCI Local Bus), but it devotes only a single paragraph to actually analyzing that Specification. In that paragraph, EMC observes that control signals (1) "control the fundamentals of all PCI data *transfers*," (2) "control[] when each phase of the transaction [*transfer*] begins and ends," and (3) are "separate[] … from command signals." *Id.* (emphasis altered) (cleaned up).

These observations are true but irrelevant. The physical layer "control signals" may well be "fundamental" *to how a transaction is transferred*, and those signals are certainly "separate … from" the transaction's "command signals." *Id.* But these observations do not suggest that these physical layer

"control signals" are *part of the transaction*. Instead, the signals are part of the transfer protocol used to communicate the transaction to its destination.

In the next paragraph (EMC Br. 31), EMC provides a string cite purporting to show that the patent specifications limit the claims to embodiments that transmit physical layer "control signals." But the text at these citations simply describes embodiments that utilize a PCI Local Bus and therefore, physical layer control signals. As ACQIS has shown (ACQIS Br. 47-49), the patent specifications also disclose embodiments that *exclude* those buses and therefore, the control signals. EMC does not even try to argue that any of the citations it provides constitute disavowal of those embodiments.

Third, EMC accuses ACQIS of telling the PTAB that PCI bus transactions must include physical layer control signals. EMC Br. 31-34. It says that ACQIS made that concession to "overcome invalidity" and is now changing position "'like a nose of wax'" to pursue infringement. *Id.* at 33.

That is completely false. ACQIS never argued to the PTAB that a transaction must include physical layer control signals, and it certainly did not "overcome invalidity" on that basis. In fact, the existence or absence of physical layer control signals was never even at issue in the IPRs.

Had ACQIS really defeated the IPRs with a parallel-to-serial conversion requirement, EMC would have cited to the section of the Final Written Decisions making that holding. EMC does not because the Final Written Decisions does not make that holding. The PTAB did not rule for ACQIS because a "transaction" must include physical layer signals; it ruled for ACQIS because EMC failed to show "that any address and data bits of a PCI industry standard bus transaction exist in the [prior art]." Appx1079.

EMC again misrepresents the IPR proceedings. As ACQIS has explained many times (ACQIS Br. 59-61), ACQIS's references to "control" information during the IPR hearing referred to *command and byte enable* information, not physical layer control signals. Expert testimony establishes that this is standard industry terminology. ACQIS Br. 10 (citing Appx2473; Appx2599 (¶¶ 57, 239); Appx3419-3420 (¶ 83)).

Finally, EMC argues that even if the claims require no parallel bus on the device *initiating* the transaction, (1) they still require one on the device *receiving* the transaction (*i.e.*, on the "peripheral"), (2) that the "control signals" necessary for operating that bus must therefore be transmitted from the initiating device, and (3) that this somehow shows that those "control signals" are part of the "transaction." EMC Br. 35-36. This argument is wrong at every step.

First, a physical bus is *not* required on the receiving end. The district court's *Markman* order clearly rejected "EMC['s] attempts to read the presence of a PCI bus *on the peripheral [i.e., receiving] side* into the claim." Appx1702. In Texas, Judge Davis held that EMC "failed to show that a PCI bus 'transaction' necessarily implies the presence of a PCI 'bus.'" Appx506. EMC tried to resurrect this argument in Massachusetts by arguing (as it does here) that, even if the claims do not require a PCI bus on the initiating side, they still require a PCI bus on the *receiving* ("peripheral") side. Appx1701 ("EMC argues that its current proposal does not contradict Judge Davis's opinion, because its proposed construction only requires that a PCI bus is involved, not that it be an 'originating' or 'intervening' PCI bus."). The district court rejected that argument, holding squarely that "the claim language does not suggest that the presence of a PCI bus [on the receiving side] has any relevance." Appx1702. EMC has not cross-appealed that construction, so no PCI Bus is required on the receiving device.

Second, even if a PCI Bus *were* required on the receiving device, EMC has not shown that this feature would require the "control signals" for that bus to be transmitted from the initiating device. The record contains no factual findings on this point.

Third, even if a PCI Bus were required on the receiving device *and* the "control signals" for that bus had to be transmitted from the initiating device, that would still not speak to the dispositive question, which is whether those "control signals" are *part of the "transaction."* They would still be part of the Specification's *physical* layer.

b) Parity Signals

EMC has less to say about the need for parity signals. EMC Br. 38-40. *First*, EMC observes that the PCI Specification describes the parity signals as mandatory ("not optional"). *Id.* at 38 (quoting Appx2332). But EMC does not explain why this means that these bits should be considered a mandatory part *of the "transaction"* rather than a mandatory part of the physical layer.

Second, EMC argues the parity signals should not be described as part of a "physical" layer because they do not control the physical medium, but instead serve a different transport function (*i.e.*, ensuring that the transaction was transmitted correctly). *Id.* This quibble over taxonomy does not change matters. Like the control signals, the parity bits play a *transport* function (*i.e.*, they are used in *transporting* the transaction from one device to another). Appx3403 (¶ 37). As ACQIS's expert opined, because "the parity

bit itself provides a transport function, [it] is *not* part of the transaction." *Id.* (emphasis added).

Third, EMC argues that a parity signal must be part of the "transaction" because it "is sent after *each* address and data phase," and therefore, excluding it would "split a PCI bus transaction … into pieces." EMC Br. 39.

EMC does not explain why a transaction cannot be sent in pieces. In fact, transactions communicated across a PCI Local Bus *are* sent in pieces (*i.e.*, in "phases"). ACQIS Br. 5-7.

EMC also fails to point to any supporting evidence or explain (or identify evidence explaining) why transport control data cannot be sent in between the pieces of the transaction without being part of the "transaction." When people have a video conversation, for example, their computers exchange many transport control messages during the conversation. That does not render those messages a part of the conversation.

It is therefore unclear why EMC thinks that transmitting parity bits between pieces of a transaction "clearly demonstrates that parity signals must be included in a PCI bus transaction." EMC Br. 40. The parity bits can be transmitted at any time without becoming a part of the transaction.

c) Phases

EMC closes by arguing that any construction of "PCI bus transaction" must require that the transaction be communicated in phases because that is how the PCI Local Bus communicates transactions. EMC Br. 40.

But the district court's *Markman* order did not require that transactions be communicated in phases. For example, the district court's construction of "communicating … [a] PCI bus transaction" (*i.e.*, "communicating a PCI bus transaction, including all address, data, and control bits") mentions only the content of the transaction, not the manner of communicating it. Appx1700-1704. EMC did not cross-appeal that holding either.

A "PCI bus transaction" is the information sent from one PCI device to another—not the manner in which that information is sent. Appx3401-3603 (¶¶ 32-36). As ACQIS's expert opined, a "POSA would understand that because phase timing is a requirement specific to the physical PCI Local Bus that [phases] are not required" when that physical bus is absent. Appx3401 (¶ 32). The record contains no contrary fact finding, which would be inappropriate at summary judgment anyway. The claims therefore do not require transmitting a PCI bus transaction in phases.

C. The Address and Data Claims should be treated separately.

ACQIS has argued that "[e]ven if the district court had correctly interpreted 'PCI bus transaction' to require the physical layer control and

parity signals (it did not), this still would not justify summary judgment of non-infringement against the Address and Data Claims because those claims recite explicitly that only the 'address and data bits of [that] … PCI bus transaction' are communicated." ACQIS Br. 53-54.

EMC offers two responses: (1) that ACQIS forfeited its argument by failing to raise it at claim construction or summary judgment, and (2) even if the Address and Data Claims only require transmitting "address and data bits," they still require *generating* a complete transaction from which to obtain those bits. EMC Br. 45-49. Both arguments are wrong, and the second is irrelevant to boot.

1. ACQIS did not forfeit its argument regarding the Address and Data Claims.

EMC argues that ACQIS forfeited its argument regarding the Address and Data Claims because "ACQIS never asked the district courts to treat th[ose] claims differently for purposes of claim construction or infringement." EMC Br. 45.

That is not how EMC saw it at the time. Here is *EMC's own claim construction brief*:

> ACQIS also argues that because some claims recite that "address and data bits of PCI bus transaction" must be communicated, those claims should not be construed to require communicating more than those bits (e.g., control bits).

Appx1393; *see* Appx1178 (ACQIS's brief).

Here is EMC's other claim construction brief:

> ACQIS suggests that, because some of the claims have language modifying the phrase "PCI bus transaction" (e.g., "*address and data bits* of PCI bus transaction," "*data* of PCI bus transaction," and "PCI bus transaction *address and data*"), fewer than all the bits of an entire PCI bus transaction could be conveyed.

Appx1141.

EMC at the *Markman* hearing:

> Their main point is well, some of the claims, some of them only say address and data bits of the PCI bus transaction. So they say those claims you shouldn't have to include control bits.

Appx1531 (116:13-16).

It seems that EMC had little trouble recognizing ACQIS's argument at the time. The argument might have even seemed familiar, given that it was *EMC's position* before it wasn't. Here is EMC at the PTAB:

> [For the Address and Data Claims] all you need to communicate are address and data bits of PCI bus transaction …. You don't have to have the complete transaction. You don't have to have the complete configuration file that a PCI bus transaction might have. You don't need the command information or the byte enables. That's not what they chose to claim.

Appx1010-1011 (13:25-14:10); *see also* Appx970.

At summary judgment, ACQIS repeated that "many claims state precisely what must be communicated, namely *only the address and data bits*

of a PCI bus transaction." Appx3337 (emphasis added) (citing '873 patent at cl. 61; '468 patent at cl. 29; '171 patent, at cl. 24).

EMC is therefore wrong that "ACQIS never asked the district courts to treat [the Address and Data Claims] differently for purposes of claim construction or infringement." EMC Br. 45. ACQIS did so at both stages.

2. EMC is also wrong that the Address and Data Claims require a full PCI Bus Transaction.

EMC argues that, even if the Address and Data Claims require sending only "address and data bits," those bits "cannot exist or be communicated without there first being a complete PCI bus transaction" on the sending device. EMC Br. 46-49. EMC reasons that "a piece of pie" (*i.e.*, the address and data bits) "cannot exist without there first being a whole pie" (*i.e.*, a full transaction). *Id.*

This analogy is tasty but flawed. The crust of a pie *can* exist without there first being a whole pie (check the freezer aisle), and the address and data bits of a PCI bus transaction can exist without there first being a whole PCI bus transaction. The PCI Standard "define[s] different address spaces and different address formats to be used when communicating a PCI Bus transaction over the PCI bus." Appx2470-2471 (¶ 51). A computer that communicates a PCI address and data bits that conform to this format and target these address spaces is communicating "address and data bits of a PCI bus transaction," as the Address and Data Claims require.

EMC argues that ACQIS itself had represented "that *all* asserted claims still require generating a full PCI bus transaction (including control bits)." EMC Br. 48-49. But EMC cites nothing to substantiate this. Instead, it cites ACQIS's argument that the Address and Data Claims exclude "ACK" transactions, which lack address bits. *Id.* It cites no evidence why that observation even suggests that the claims "require generating a full PCI bus transaction (including control bits)." *Id.* at 49.

II. "Communicating … [a] PCI bus transaction" should be given its ordinary meaning.

There appears to be no dispute that the phrase "communicating … [a] PCI bus transaction" carries its ordinary meaning (in light of the construction of "PCI bus transaction"). ACQIS argued for that construction in its opening brief (ACQIS Br. 57-61), and EMC has not disagreed.

EMC touches on the "communicating" term only fleetingly, and only to argue that "communicating … [a] PCI bus transaction" requires communicating *all* the bits of that transaction. EMC Br. 37. But there is no dispute on that score. The dispute is only whether all the bits *of a transaction* include physical layer signals (as EMC contends). That dispute is resolved by construing a "PCI bus transaction." Because there is no dispute that "communicating" a transaction should carry its ordinary meaning, the Court should make that holding.

III. "Encoded … (PCI) bus transaction" does not require parallel-to-serial conversion.

Finally, EMC is wrong that (1) the district court's construction of "encoded" provides a second, independent ground for affirmance, and (2) the construction is correct to require an "encoded" serial transaction to have always been converted from *parallel signals* (rather than simply created from data in memory). EMC Br. 50-60.

A. The construction of "encoded" is not an alternative ground to affirm the judgment.

The district court's construction of "encoded" does not "provide[] an independent, or alternative, ground for affirming the judgment." EMC Br. 56; *see also id.* at 55-60.

Contrary to EMC's argument, the summary judgment order does *not* hold that ACQIS failed to show that the accused products "encode" a "PCI bus transaction" "under *any* construction of ['PCI bus transaction']." *Id.* at 59 (emphasis added). Rather, the order holds that the information that the accused products do "encode" *is not a "PCI bus transaction," under the district court's erroneous construction of that term*. Appx11-12 (emphasis added). Because this reasoning turns entirely on the district court's construction of "PCI bus transaction," it is not an "independent, or alternative, ground for affirming." EMC Br. 56.

EMC argues that this understanding of the order "blinks reality." EMC Br. 59. But it is EMC who stares reality in the face and denies it. The

order's reasoning is clear. The district court construed "encoded" to require "serializ[ing] from a parallel form." Appx11. At summary judgment, "ACQIS respond[ed] that the accused products do serialize data from parallel form." *Id.*; *see also* Appx3362-3364; Appx2587-2593; Appx3406-3417. The district court *agreed*, but it held that the serialized data ACQIS had identified *"is not communicated as a PCI bus transaction"* specifically because it "do[es] not include the [physical layer] *control signals*" required by EMC's erroneous construction. Appx11 (emphasis added). Thus, the district court concluded "that EMC's products modify *some data* from parallel to serial form," but that this data is not a "PCI bus transaction" *under EMC's construction of "PCI bus transaction*." Appx12.

Because the district court's reasoning with respect to "encoded" turns entirely on its erroneous interpretation of "PCI bus transaction," that reasoning is not "an independent, or alternative, ground for affirming the judgment." EMC Br. 56. That is also why ACQIS need not "dispute [on appeal] that under [the district court's] construction [of 'encoded'], the accused products do not infringe" (*id.*): the district court never made that holding, so ACQIS cannot appeal it.

EMC argues that this Court can find non-infringement in the first instance (even under ACQIS's construction of "PCI bus transaction") because "ACQIS failed to present evidence" of infringement under the district court's

construction of "encoded," so there is no "genuine issue of material fact on this point." *Id.* at 56-57.

That contention is outright false. At summary judgment, ACQIS presented evidence that the accused products serialize a "PCI bus transaction," under ACQIS's construction of that term. Appx3362-3364; Appx2587-2593; Appx3406-3417. For example, ACQIS's summary judgment brief explained how "the Accused Products serialize[], from a parallel form, *all address, data, command, and byte enables* of the PCI Express transaction." Appx3362-3364 (emphasis added). Moreover, ACQIS supported that argument with two lengthy expert reports explaining how the "Accused Products serialize[] PCI bus transactions from a parallel form." Appx2587-2593; *see also* Appx3406-3417. That argument and evidence answers the non-infringement arguments EMC made to the district court and repeats on appeal (EMC Br. 57).

In light of this record, it is odd for EMC to argue that "ACQIS failed to present evidence that the accused products serialize a PCI bus transaction (*however construed*) or raise any genuine issue of material fact on this point." EMC Br. 56-57 (emphasis added). That is flatly untrue, and the district court never held so. Consequently, if the Court modifies the construction of "PCI bus transaction," it should vacate the district court's holding that the accused products do not "encode" such "PCI bus transactions" and

remand with instructions to resolve that issue in the first instance, in light of the correct construction of "PCI bus transaction."

B. The district court misconstrued "encoded."

If the Court clarifies the construction of "PCI bus transaction" and remands the infringement issue to the district court, it should also correct the district court's erroneous requirement that "encoding" a transaction demands converting it to serial form *from parallel signals* (rather than from data in memory).

As ACQIS explained (ACQIS Br. 62-68), the district court imposed that requirement based solely on a prosecution disclaimer that never occurred. Rather than rehabilitate the district court's reasoning, EMC simply repeats the district court's mistakes and piles on more misrepresentations about the record. EMC Br. 50-55.

1. ACQIS made no disclaimer.

EMC is wrong that ACQIS made any disclaimer regarding "encoded" during the IPRs. EMC Br. 50-53. EMC again misrepresents that ACQIS somehow won the IPRs by showing that the prior art failed to create serial transactions *from parallel signals* (rather than, for example, from data in memory). EMC Br. 50-53. That contention is just plain false. Parallel-to-serial conversion played *no role* in the IPR decisions, and ACQIS never argued that it should. ACQIS Br. 63-68. To the contrary, ACQIS argued that

encoding does *not* require converting parallel signals, and it even conceded that the prior art "encoded" transactions without that feature. *Id.*

a) Parallel-to-serial conversion played no role in the IPR decisions.

EMC's IPRs did not fail because the prior art lacked parallel-to-serial conversion. ACQIS Br. 63-64. Indeed, neither Final Written Decision faults the prior art for lacking that feature. *See*, *e.g.*, Appx1064-1108. Instead, each faults the prior art for failing to transmit "PCI bus transactions" and instead, transmitting "TNet transactions" and "CPU transaction[s]":

> Petitioner does not identify persuasive evidence indicating that either the CPU transaction or the TNet transaction is a PCI industry standard bus transaction. Thus, the evidence identified in the Petition *does not indicate that the information output by the TNet processor interface over the TNet links includes address and data bits of a PCI industry standard bus transaction in serial form*.

Appx1075-1076 (emphasis added) (citations omitted). This reasoning has nothing to do with whether anything is converted from parallel signals, and everything to do with EMC's failure to show that the "TNet transaction … includes any data bits of a PCI industry standard bus transaction" or "any address bits of a PCI industry standard bus transaction." Appx1077.

b) ACQIS never tried to distinguish the prior art based on parallel-to-serial conversion.

EMC is also wrong that ACQIS "distinguished the prior art based on the parallel-to-serial conversion requirement." EMC Br. 53. In support,

EMC references ACQIS's statements that the prior art "never used a serialized PCI bus transaction, only parallel." *Id.* (citing Appx783).

That statement has nothing to do with a parallel-to-serial conversion requirement. The prior art transmitted "TNet transactions" over a serial interface, and the receiving device used those TNet transactions to create parallel PCI bus transactions. Appx1075-1076. ACQIS therefore argued that this prior art "never used a serialized PCI bus transaction, only parallel." Appx783. This argument does not even suggest that a "serialized PCI bus transaction" must be created from parallel signals rather than from any other source (*e.g.*, from data in memory).

EMC also rehashes the same oral argument quotations on which the district court relied (EMC Br. 50-53), but as ACQIS already explained (ACQIS Br. 65-68), each quotation was taken out of context to alter its meaning. The patented idea is to transmit PCI transactions more quickly by doing so *serially* rather than by using the traditional *parallel* method. That is all ACQIS intended to convey when it explained that the invention boosts speeds "**by making the PCI communication serial rather than parallel**" or that "**one key to the invention [i]s to serialize the otherwise parallel PCI bus transactions**." EMC Br. 50-51 (citing Appx786 and Appx782) (emphasis altered). Each of these statements merely compares the inventors' improvement (*i.e.*, serialized communication) to the prior art

(*i.e.*, parallel communication). None suggests that the invention must create the serial transactions *from parallel signals*.

The context of each statement confirms this. For example, consider ACQIS's representation that "'**the whole point' of the claimed invention was … 'going from parallel'** [to serial]." EMC Br. 51-52 (emphasis altered) (discussing Appx1026-1028). The statement was a side comment about the invention in general, made during a discussion that had nothing to do with parallel-to-serial conversion: ACQIS was responding to a question about whether the prior art used PCI address formats, not whether the prior art serialized *parallel signals*.

The other statements on which EMC relies are even weaker. That the invention "***use[s] the existing PCI standard***" and that the standard traditionally employs "***parallel*** communications" (EMC Br. 51) (citing Appx789-790) simply means that the invention communicates transactions that comply with the standard and that those transactions were traditionally communicated in parallel. It does not suggest that the invention must create those transactions from parallel signals.

Weakest are EMC's citations to an IPR deposition transcript, where ACQIS's technical expert appeared to agree that "the claims, in your reading, contemplate some sort of ***transformation of the PCI bus transaction into a format that is serially transmitted.***" EMC Br. 51 (quotation completed) (citing Appx923-924). Deposition testimony of an expert witness

cannot establish prosecution disclaimer because it is "the *patentee's* words that define the claim" (not a fact expert's comments at a deposition), and EMC has not shown that ACQIS adopted the expert's deposition statement. *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1332 (Fed. Cir. 2013).

In sum, ACQIS described "the whole point" of its invention as transmitting PCI bus transactions in serial form rather than in the traditional parallel form. EMC Br. 52 (citing Appx1027). That is not an admission that the invention requires serializing the transactions *from parallel signals*.

c) ACQIS argued that encoding does not require parallel-to-serial conversion and conceded that the prior art "encoded" without it.

As ACQIS has explained (ACQIS Br. 63-64), disavowal is particularly inappropriate in view of the entire prosecution history. "[T]he '*totality* of the prosecution history' informs the disavowal inquiry." *Comput. Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008) (emphasis added). And here, that history includes ACQIS arguing expressly that "encoding" does *not* require parallel-to-serial conversion (Appx798-799) and even *conceding* that the prior art "encoded" transactions without performing parallel-to-serial conversion (Appx817; Appx1099-1100; Appx1104 n.4).

Specifically, ACQIS proposed that "encoding" can be any of three types of operations described in the patent specifications: operations that "(1) turn[] … signal[s] into bits, (2) group[] bits into a specified size block, or

(3) order[] bits onto one or more serial transmission lines." Appx799. ACQIS then conceded that the prior art satisfies the "encoded" limitation under the second option, which does not describe parallel-to-serial conversion. ACQIS Br. 64 (citing Appx817).

Expert testimony confirmed that this second type of encoding does not require parallel-to-serial conversion. Appx1223-1225 (¶ 123) ("[o]nly one of the[se] types of encoding identified in the Acqis patent specifications—(1) turning PCI bus signals into bits—is related to parallel-to serial conversion from a physical PCI bus"). And *EMC* even conceded that this type of encoding "is not parallel-to-serial conversion." Appx1782 (¶ 57). In light of this history, it is difficult to imagine how a few side-comments at the IPR hearing could possibly constitute "clear and unmistakable" disavowal. *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012).

EMC argues that the construction ACQIS proposed at the PTAB does not undermine EMC's disclaimer argument because "'group[ing] bits into a specified size block'" could "*involve* parallel-to-serial conversion." EMC Br. 53. (emphasis added). In support, EMC notes that "parallel to serial converters" can convert a parallel signal "into 10 bit packets." EMC Br. 54 (citing Appx152, 1710).

That argument is illogical. That parallel-to-serial converters can arrange data into 10-bit packets does not mean that arranging data into 10-

bit packets requires parallel-to-serial converters. Data in memory can be arranged into 10-bit packets just as well. ACQIS's concession that "encoding" comprises *any* function that "group[s] bits into a specified size block" (Appx799) therefore means that the claims do not require parallel-to-serial conversion.

2. The specifications do not require parallel-to-serial conversion.

EMC also argues that the district court's parallel-to-serial requirement "did not rely solely on its disclaimer finding," but "independently" on the patents' specifications. EMC Br. 53-54. That is wrong. The district court did not hold that the specifications contain an independent disclaimer—only that they are "*consistent with* an interpretation requiring parallel-to-serial conversion." Appx1709 (emphasis added).

The district court found no disclaimer in the specifications because none exists. To the contrary, the specifications disclose embodiments without parallel buses and therefore, no parallel-to-serial conversion. ACQIS Br. 13-15; Appx1700-1705; Appx1220-1223. Those parts of the specifications that were "consistent with" parallel-to-serial conversion (Appx1709 and EMC Br. 54) simply describe embodiments with parallel buses and therefore, parallel-to-serial conversion. The specifications provide no "independent[]" disclaimer requiring parallel-to-serial conversion. EMC Br. 53.

3. PCI bus transactions are not inherently parallel.

Finally, EMC accuses ACQIS of ignoring the surrounding claim language, which requires encoding a *"PCI bus transaction."* EMC Br. 54-55. EMC argues that "encod[ing]" a "PCI bus transaction" *always* requires converting the transaction from parallel signals because a "PCI bus transaction" is *always* parallel signals. EMC Br. 54-55.

This argument is self-contradictory. That a "PCI bus transaction" can be encoded into serial form is alone sufficient proof that a "PCI bus transaction" need not always be parallel signals. Indeed, the entire purpose of the invention is for the "PCI bus transaction" to be transmitted in *serial* form. Clearly then, a "PCI bus transaction" *can* exist in a form other than parallel signals. As Judge Davis held, a "PCI bus transaction" is merely the "information in accordance with the PCI standard." Appx506-507. There is no reason why that information must be encoded from parallel signals, rather than simply from data in memory. *Id.*

CONCLUSION

The Court should vacate the district court's grant of summary judgment and remand to consider ACQIS's argument on the construction of "PCI bus transaction." Alternatively, the Court can hold that a "PCI bus transaction" does not require the physical layer elements on which the district court relied and reverse or vacate. The Court should also hold that (1) "communicating" carries its ordinary meaning, and (2) Judge Davis's construction of "encoded … (PCI) bus transaction" is correct.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to Federal Rule of Appellate Procedure 32(g), the undersigned counsel for Appellee certifies that this brief:

(i) complies with the type-volume limitation of Federal Circuit Rule 32(b)(1) because it contains 6,877 words, including footnotes and excluding the parts of the brief exempted by Federal Circuit Rule 32(b)(2) and Federal Rule of Appellate Procedure 32(f); and

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Dated: January 28, 2022

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